THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte MITSUHIRO TAKAHASHI,
SEIJI TATEYAMA, and
MASAHIDE TOMITA

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Appeal No. 96-1727
Application 08/130,575[1]

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HEARD: April 7, 1999

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Before THOMAS, DIXON, and FRAHM, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 and 4 through 9, which constitute all the claims in the application.

[1] Application for patent filed October 1, 1993.

Representative claim 1 is reproduced below:

1. An image processing system, comprising:

a processor side memory for storing image data to be processed;

processor means, coupled to the processor side memory, for processing the image data supplied from the processor side memory;

a display side memory for storing the image data transmitted from the processor means;

control means for controlling transmission of the image data from the processor means so that the image data are transmitted for each unit of predetermined rasters to the display side memory;

encoder means for encoding the image data supplied from the display side memory to form display signals; and

display means responsive to the encoder means for displaying images corresponding to the display signals for each unit of the predetermined rasters.

The following reference is relied on by the examiner:

Nishi et al. (Nishi)	4,897,636	Jan. 30, 1990

Claims 1 and 4 through 9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nishi.

Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.

OPINION

Because we have difficulty in following the examiner's correlation of the claimed features to Nishi, difficulty in agreeing with the examiner, and in part due to our agreement with some of appellants' views as to this correlation, we reverse the outstanding rejection of all claims on appeal under 35 U.S.C. § 102 as set forth by the examiner. However, we institute our own rejection under the provision of 37 CFR § 1.196(b) as set forth below.

Claims 1, 4, 8, and 9 are rejected under 35 U.S.C. § 102 and, in the alternative, under 35 U.S.C. § 103 over Nishi alone.

The subject matter of independent claim 1 on appeal appears to be met by the teachings at columns 1 and 2 under 35 U.S.C. § 102 and clearly would have been obvious over Nishi's admitted prior art with respect to Figures 1 and 2. The claimed processor side memory for storing image data to be processed comprises the data memory 103 in prior art Figure 1 where the processor means recited is met by the CPU 102 which does in fact process the image data supplied from that memory for placement into the VRAM 104 through the video data processor VDP 101 before the display means claimed presents the information on CRT 105. According to the teachings of Nishi regarding Figure 1, the CPU 102 and/or the VDP 101 may control the processing and storing of image data transmitted from the processor CPU 102. The VDP 101 comprises the claimed control means since it

clearly controls transmission of image data from a processor means to the claimed display side memory represented by VRAM 104. The processing occurs in units of the broadly defined predetermined rasters, to the extent claimed, as depicted in the data blocks R1 and R2 in prior art Figure 2. In accordance with the discussion bridging columns 1 and 2 of Nishi, the color processing would entail the teaching corresponding to the claimed encoder means.

Even with respect to both the Figure 3 and Figure 20 embodiments of Nishi's own teachings, the claimed processor side memory of claim 1 may comprise the memory 3 where the processor means recited comprises the CPU 2. In Nishi's Figure 3 the VRAM clearly stores information transmitted to it from the CPU through the VDP 1. It is this VDP 1 that comprises the claimed control means which controls the transmission of image data from the processor means CPU 102 in Figure 3 of Nishi so that image data are transmitted for each unit of predetermined rasters to display side memory VRAM 4. Again, the context of the whole disclosure of Nishi is to process data blocks in a manner similar to the data blocks for image presentation depicted in prior art Figure 2 as represented in succeeding figures. Some of the details of identifying the addressability of each of these blocks relate to Figures 4 through 7 of Nishi. See also Figures 11, 12, and 14. In accordance with Figure 3 the details of the control means may further comprise the command processing circuit 15 and the image and data processing circuit 10, whereas

the claimed encoder means may comprise the color palette circuit 12 which encodes for color presentation bit data supplied to it from the VRAM 4 to form display signals to be imparted to the CRT 5, which unit again displays the data in the claimed "units of predetermined rasters."

The Figure 20 version, as principally relied upon by the examiner, may additionally be construed to teach that the VRAM 4 and the extended VRAM memory 80 may comprise the display side memory. The claimed processor side memory of claim 1 is not recited in such a manner as to exclude the external supply memory 3 as comprising this memory for purposes of this claim. It is further noted that with respect to the admitted prior art discussion of Figures 1 and 2 as discussed at the top of column 2 of Nishi, it was known in the art that the VRAM may also be extended by an additional memory device in the manner depicted with respect to Figure 20.

As to claim 4, the original memory 3 in the Figure 3 version of the embodiments in Nishi reads upon the claimed external storage means of the preamble of claim 4 and the CRT 5 remains the display monitor means of this claim. The first memory means comprises alternatively the VRAM 4 and the extended VRAM memory 80 of the Figure 20 embodiment whereas these same memories, because of their functional usages with respect to the Figure 20 embodiment, also may be construed to comprise the second memory means claimed. The VRAMs 4 and 80 clearly are taught to buffer image data

transmitted from a source memory 3 in the Figures 3 and 20 embodiments. The claimed control unit in claim 4 reads upon the CPU 2 which is coupled to this previously recited external memory 3 and to the VRAMs 4 and 80 as just discussed and the CPU clearly processes image data stored in the VRAMs 4 and 80. Again, in the context of the disclosure in Nishi as a whole, the processing occurs in the claimed units of predetermined rasters such as first introduced in prior art Figure 2 in Nishi. The claimed image data extension unit performs a decoding function met by the details of the video data processor 1 including optionally the command processor circuit 15,15a; the image data processing circuit 10,10a in the Figures 3 and 20 embodiments. These two units work together to perform the logical operations upon the video data to the extent necessary in Nishi. As such, they perform the claimed decoding operation as broadly recited. Because the CPU 2, the command processing circuit 15, and the image data processing circuit 10 shuttle data in and out of the VRAMs 4 and 80 they may be clearly construed to store decoded image data that had been operated upon in accordance with these logical operations at least with respect to element 15 in Nishi. The claimed means for transmitting data functionally reads upon the functions provided by the image data processing circuit 10 and the color palette circuit 12, which unit clearly meets the video encoder unit feature of dependent claim 9 on appeal.

Because the CPU 2 is in overall control over the entire operation, it necessarily includes or would have been obvious to include the claimed data start register means for controlling the transmission start timing of the image data for each unit of stored rasters, that is, for each region for which image data will be moved, in accordance with the data block movement figures of Nishi such as Figure 2. Necessarily inherent within the artisan's understanding of the manner in which raster scanned devices such as CRT unit 5 operates in Nishi and obvious in view of this understanding, particular regions such as defined in Nishi's prior art Figure 2 to be moved are clearly identified based upon the raster scanned position set forth by X and Y addressibilities within the noted memories. The address from which data is to be read or to be written into in a given transfer operation necessarily determines the positional location of the image to be moved on the video display 5. See again Figures 4 through 7, 11, 12, and 14.

With respect to the features of dependent claim 8, the discussion of prior art Figure 1 at column 1 in Nishi indicates that both still and animation patterned images are to be displayed in the context of video games. The title of Nishi clearly indicates that Nishi's device is directed to moving display images. Even the arrow between the image locations R1 and R2 indicates that there is a vertical movement or scrolling action to the extent recited in dependent claim 8 on appeal even in the prior art of Nishi.

We do not set forth a rejection for dependent claims 5 through 7 since Nishi clearly does not teach the features recited therein. The VRAM memories in Nishi are not taught to be used alternatively since there is no specific teaching that two RAM's are used in an alternate manner to increase the process speed of the image data as recited in dependent claim 5. There is no specific teaching that two RAMs perform alternatively read and write operations to so increase the speed of image data. As such, the features of its dependent claim 6 also cannot be met by Nishi. Additionally, since there is no teaching in Nishi of data compression or decompression in a video display environment, the features recited in dependent claim 7 cannot be met. The examiner may choose to apply additional prior art to Nishi to reject claims 5 through 7.

It is noted that there are additional VRAM teachings in the options paragraph at column 29 beginning at line 46 which expand even further the interpretation of the various dual memories recited in each independent claim on appeal beyond those specifically set forth and noted. To the extent broadly recited in the noted claims that we reject, the identified elements in Nishi appear to be identical to or correspond in structure and function to the claimed elements that are rejected.

It is thus believed that the bulk of the appellants' arguments in the brief and reply brief directed at Nishi have been answered directly or indirectly by the above noted correlation. With respect to appellants' arguments at pages 11 and 12 of the principal

brief on appeal relating to the image data extension unit recitation in independent claim 4 on appeal, we generally agree with the examiner's response as set forth at pages 9 and 10 of the answer. It goes without saying that the image data extension unit is not recited in means-plus-function format in this claim and the examiner has clearly pointed out in addition to our own above correlation that the claimed decoding function is met by the reference. There is no recitation in this claim that any compression/ decompression operations occur.

In summary, we have reversed the examiner's rejection of claims 1 and 4 through 9 and instituted our own rejection under 35 U.S.C. § 102 and, alternatively, under 35 U.S.C. § 103 of claims 1, 4, 8, and 9 in view of Nishi alone.

This decision contains a new ground of rejection pursuant to 37 CFR §.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with

respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .
>
> (2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED - 37 CFR § 1.196(b)

JAMES D. THOMAS Administrative Patent Judge	)
JOSEPH L. DIXON Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
ERIC S. FRAHM Administrative Patent Judge	)

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